## REMARKS

This Amendment responds to the Office Action dated October 5, 2004 in which the Examiner rejected claims 15 and 19 under 35 U.S.C. §112, second paragraph, and rejected claims 1-20 under 35 U.S.C. §103.

As indicated above, a minor informality in the specification has been corrected. Applicants respectfully request the Examiner approves the correction.

As indicated above, claim 19 has been amended to delete the words "for example". However, no such wording appears in claim 15. Therefore, applicants respectfully request the Examiner withdraws the rejection to claims 15 and 19 under 35 U.S.C. §112, second paragraph.

As indicated above, the claims have been amended in order to make explicit what is implicit in the claims. The amendments are unrelated to a statutory requirement for patentability.

Claims 1-20 were rejected under 35 U.S.C. §103 as being unpatentable over *Tsuto* (U.S. Patent No. 6,138,295) in view of *Green et al* (U.S. Patent No. 4,965,799).

*Tsuto* appears to disclose an improved semiconductor memory testing apparatus which is provided with a plurality of pattern generators and capable of testing high-speed semiconductor memories in addition to normal speed semiconductor memories. (col. 1, lines 9-13) FIG. 4 illustrates in block form the general configuration of a semiconductor memory testing apparatus which employs the high-speed pattern generator shown in FIG. 1. In FIG. 4 the components or parts corresponding to those in FIG. 7 are identified by the same reference numerals. The pattern generator 11 has the pattern generation parts 21A and 21B as discussed

previously with respect to FIG. 1, which generate pattern data D1, D3, D5, . . . and D2, D4, D6, . . . shown in FIGS. 5A and 5B, respectively. The pattern data D1, D3, D5, . . . and D2, D4, D6, . . . are converted by the high-speed conversion part 16 to obtain a high-speed pattern data D1, D2, D3, D4, D5, . . . having a frequency of twice that of the pattern data, as shown in FIG. 5C. The high-speed pattern data D1, D2, D3, D4, D5, . . . are inputted to the waveform shaping part 12 where they are converted to a high-speed pattern signal having real waveforms (in analog form), which in turn are applied to the memory under test DUT to be written therein. The memory under test DUT is read out at the same rate or speed as that of writing therein, and hence a high-speed read-out signal R1, R2, R3, R4, R5, . . . shown in FIG. 5D is outputted from the memory under test DUT. The high-speed read-out signal R1, R2, R3, R4, . . . is converted by a low-speed conversion part 17 into two low-speed read-out signals R1, R3, R5, . . . and R2, R4, R6, . . . shown in FIGS. 5E and 5F, respectively, which in turn are supplied to logical comparison parts 13A and 13B, respectively. The logical comparison parts 13A and 13B are supplied with low-speed expected value signals (expected value pattern data) E1, E3, E5, . . . and E2, E4, E6, . . . shown in FIGS. 5G and 5H, respectively, from the corresponding ones of the two pattern generation parts 21A and 21B of the pattern generator 11, for logical comparison with the above-mentioned low-speed read-out signals R1, R3, R5, . . . and R2, R4, R6, . . . . This embodiment has been described to use the two logical comparison parts 13A and 13B, but the logical comparison could also be made by one high-speed logical comparison part which operates at high speed or rate as in the case of FIG. 7. In such an instance, the low-speed conversion part 17 is unnecessary and the high-speed pattern data (FIG. 5C) obtained from the high-

speed conversion part 16 can be used as the expected value signal. While in the above the two pattern generation parts 21A and 21B are shown to be controlled by the common single sequence control part 100, more than two pattern generation parts can be used. The larger the number of the pattern generation parts, the faster or higher in speed the pattern generator can be obtained. (col. 11, lines 11-61)

Thus, *Tsuto* merely discloses pattern data are converted by high speed conversion part 16 to obtain a high speed pattern data which is then input to a device under test, the DUT outputs high speed readout signal which is converted by a low speed conversion part 14 into low speed readout signals and supplied to comparison parts 13a and 13b. Thus nothing in *Tsuto* shows, teaches or suggests a) a data transferring apparatus which operates at a low frequency while input and output data are provided at full frequency as claimed in claim 1, b) operations of data transfer are performed at a low frequency while input and output data are provided at full frequency as claimed in claim 10 and c) an algorithmic pattern generator and fault logic devices operate at low frequency while registers access the device under test at full frequency as claimed in claim 18. Rather, *Tsuto* merely discloses a pattern generator 11 which outputs pattern data which is converted to high speed pattern data, the high speed data is input to a device under test and the output of the device under test is converted to low speed data.

*Green et al* appears to disclose a variable clock 10 sets the operational speed of the apparatus by providing a variable clock signal to a timing generator 20 which generates row access strobe (RAS), column access strobe (CAS) and sequencing signals to a test socket 50 into which a chip to be tested is inserted, and to row and column address counters 30 and 40 respectively. The clock 10 also provides a clock

signal to random sequencer 60, which generates unique pseudo-random data bit patterns to be written into the DRAM under test. (col. 2, lines 31-42) The variable clock control allows the user to adjust the speed at which the DRAM is tested to determine the maximum or minimum speed at which the DRAM will operate properly. (col. 3, lines 9-12)

Thus, *Green et al* merely discloses a variable clock. However, nothing in *Green et al* shows, teaches or suggests a) a data transferring apparatus operates at a low frequency while input and output data are provided at full frequency as claimed in claim 1, b) operations of data transfer are performed at low frequency while input and output data are provided at full frequency as claimed in claim 10, or c) an algorithmic pattern generator and fault logic device is operated at low frequency while registers access the device under test at full frequency as claimed in claim 18. Rather, *Green et al* merely discloses a variable clock.

Since neither *Tsuto* nor *Green et al* shows, teaches or suggests the primary features as claimed in claims 1, 10 and 18, applicants respectfully request the Examiner withdraws the rejection to claims 1, 10 and 18 under 35 U.S.C. §103.

Claims 2-9, 11-12, 14-17 and 19-20 depend from claims 1, 10 and 18 and recite additional features. Applicants respectfully submit that claims 2-9, 11-12, 14-17 and 19-20 would not have been obvious within the meaning of 35 U.S.C. §103 over *Tsuto* and *Green et al* at least for the reasons as set forth above. Therefore, applicants respectfully request the Examiner withdraws the rejection to claims 2-9, 11-12, 14-17 and 19-20 under 35 U.S.C. §103.

The prior art of record, which is not relied upon, is acknowledged. The references taken singularly or in combination do not anticipate or make obvious the claimed invention.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is respectfully requested to contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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